# A Comparison of the INS8250, NS16450 and NS16550AF Series of UARTs

National Semiconductor
Application Note 493
Martin S. Michael
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National currently produces seven versions of the INS8250 UART. Functionally, these parts appear to be the same, however, there are differences that the designer and purchaser need to understand. For each version, this document provides a brief overview of their distinct characteristics, a detailed function and timing section, a discussion of software compatibility issues and the AC timing parameters.

## 1.0 Part Summary

The seven versions currently produced are designated INS8250, INS8250-B, INS8250A, NS16450, INS82C50A, NS16C450, and NS16550AF. These devices are grouped below by process type.

**XMOS DEVICES**

1. INS8250: This is the original version produced by National. It is the same part as the INS8250-B, but with faster CPU bus timings.
2. INS8250-B: This is the slower speed (CPU bus timing) version of the INS8250. It is used by many popular 8088-based microcomputers.
3. INS8250A: This is a revision of the INS8250 using the more advanced XMOS process. The INS8250A is better than the aforementioned parts due to the redesign (compare section 2.0 to 3.0) and the following process characteristics—closer threshold voltage control, more reliably implemented process topography and finer control over the active area critical dimensions. XMOS and CMOS parts should be used for all new designs. This part is used in many popular 8086-based microcomputers.
4. NS16450: This is the faster speed (CPU bus timing) version of the INS8250A. It is used by many popular 80286-based microcomputers.
5. NS16550AF: This is the newest member of the UART family. It powers-up in the NS16450 mode and is completely compatible with all software written for the NS16450. It has advanced features such as on-board FIFOs, a DMA interface, faster CPU bus timings and a much higher maximum baud rate than the NS16450. The NS16550AF should be used for all new non-CMOS designs, including those that were originally done with the NS16550. It is used in recent versions of popular 80286-based, 80386-based and ROMP-based microcomputers. Software written for the NS16550 is completely compatible with the NS16550AF. Section 5.0 describes how the software can distinguish between the NS16550 and the NS16550AF.
6. NS16550: This part powers-up in the NS16450 mode and is completely compatible with all software written for the NS16450. It has advanced features, such as a DMA interface. The on-board FIFOs are essentially non-functional. This part was issued on a limited basis. Any user that wants this part should order the NS16550AF. Section 5.0 describes the differences between the NS16550 and the NS16550AF in detail.

**CMOS DEVICES**

1. INS82C50A: This is a CMOS version of the INS8250A. It functions identically and for most AC parameters has the same timing specification as the INS8250A (see Section 4.0). It draws approximately 1/10 (10 mA) of the maximum operating current of the INS8250A.
2. NS16C450: This is a CMOS version of the NS16450. It functions identically and for most AC parameters has the same timing specification as the NS16450 (see Section 4.0). It draws approximately 1/12 (10 mA) of the maximum operating current of the NS16450.

**Note:** The XMOS and CMOS UARTs are not plug-in replacements for the INS8250/INS8250-B when used with ICUs that are in the popular edge-triggered configuration. However, there are easily implemented adjustments to the driving software or associated hardware that will allow these parts to be a plug-in replacement (see Section 6.0).

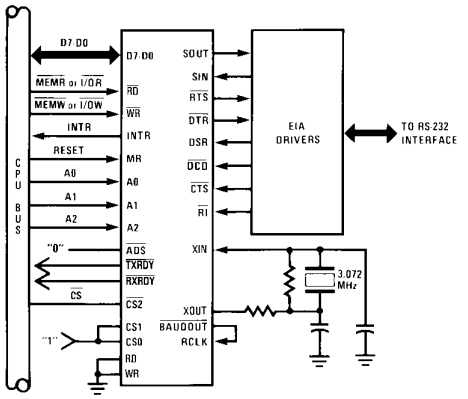


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**FIGURE 1. Connection Diagram**

## 2.0 INS8250 and INS8250-B Functional Considerations

Designers using these parts should be aware of the following considerations.

1. When multiple interrupts are pending, the interrupt line (INTR) pulses low after each interrupt instead of remaining high continuously.

   Recommendation: This will not cause problems in normal operation, however, it is a condition necessary for compatibility in some popular 8086- and 80286-based microcomputers that use an edge-triggered ICU (see Section 6.0).

 

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2. Bit No. 6 (TSRE) of the line status register is set as soon as the transmitter shift register empties whether or not the transmitter holding register contains a character. Bit No. 6 is then reset when the transmitter shift register is reloaded.

   Recommendation: This will not cause problems in normal operation. However, it is a function tested on some popular 8088-based microcomputer systems diagnostic programs.

3. In loopback mode the modem control outputs $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$ and $\overline{OUT2}$ remain connected to the associated Modem Control Register bits.

## 3.0 INS8250A and NS16450 Function and Timing Considerations

1. The loopback diagnostic function sets the modem control outputs $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$ and $\overline{OUT2}$ to their inactive state (logic ''1''), so they will send no spurious signals.
2. A one byte scratch pad register is included at location 111. This register is not on the INS8250 or -B.
3. When multiple interrupts are pending the interrupt line remains high rather than pulsing low after each interrupt is serviced. The INS8250A and NS16450 have level sensitive interrupts as opposed to edge-triggered interrupts. This requires a change in the UART driver software or associated hardware if the INS8250A, NS16450 is used with some popular microcomputers, and their edge-triggered ICUs (see Section 6.0).
4. Bit 6 of the line status register is set to 1 when both the transmitter holding and shift register are empty. This causes the INS8250A and NS16450 to be incompatible with some INS8250 software utilizing this bit.

### 3.1 TIMING CONSIDERATIONS

1. A start bit will be sent typically 16 clocks (1 bit time) after the WRTHR signal goes active.
2. The leading edge of WRTHR resets THRE and TEMT.
3. All of the line status errors and the received data flag (DR, data ready) are set during the time of the first stop bit.
4. TEMT is set 2 RCLK clock periods after the stop bit(s) are sent.
5. The modem control register updates the modem outputs on the trailing edge of WRMCR.

## 4.0 INS82C50A and NS16C450 Function and Timing Considerations

All of the information presented in Sections 3.0 through 3.2 is applicable to the CMOS parts. In addition, the following items specify differences between XMOS and CMOS parts. They are applicable to the CMOS parts only:

1. Anytime a reset pulse is issued to the INS82C50A or NS16C450 the divisor latches must be rewritten with the appropriate divisors in order to start the baud rate generator.
2. $t_{SI}$ is from 16 to 48 RCLK cycles in length

## 5.0 NS16550AF and NS16550 Function and Timing Considerations

All of the information present in Sections 3.0 and 3.1 is applicable to the NS16550AF and NS16550.

The primary difference between these two parts is in the operation of the FIFOs. The NS16550 will sometimes transfer extra characters when the CPU reads the RX FIFO. Due to the asynchronous nature of this failure there is no workaround and the NS16550 should NOT be used in the FIFO mode. The NS16550AF has no problems operating in the FIFO mode and should be used on all new designs.

The programmer should note the difference in the function of bit 6 in the Interrupt Identification Register (IIR6). This bit is permanently at logical 0 in the NS16550. In the NS16550AF this bit will be set to a 1 when the FIFOs are enabled. In both parts bit 7 of the IIR is set to a 1 when the FIFOs are enabled. Therefore, the program can distinguish when the FIFOs are enabled and whether the part is an NS16550AF or an NS16550 by checking these two bits. In order to enable the FIFO mode and set IIR6 and IIR7 bit 0 of the FIFO Control Register (FCR0) should be set. Remember unless both bits IIR6 and IIR7 are set, the program should not transfer data via the FIFOs.

The following are improvements in the AC timings for the NS16550AF over the NS16450:

1. $t_{AR}$ changes from 60 ns to 30 ns.
2. $t_{CSW}$ changes from 50 ns to 30 ns.
3. $t_{CSR}$ changes from 50 ns to 30 ns.
4. RC changes from 360 ns to 280 ns.
5. $t_{RC}$ changes from 175 ns to 125 ns.
6. $t_{DS}$ changes from 40 ns to 30 ns.
7. $t_{DH}$ changes from 40 ns to 30 ns.
8. $t_{AW}$ changes from 60 ns to 30 ns.
9. $t_{WC}$ changes from 200 ns to 150 ns.
10. WC changes from 360 ns to 280 ns.
11. Timing parameters specified by $t_{SINT}$ will change in some cases when the FIFOs are enabled. Refer to the data sheet for specific changes.

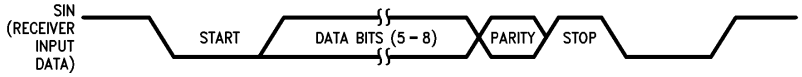


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**FIGURE 2. Serial Data Timing**

## 6.0 Software Compatibility

Two of the conditions present in the INS8250-B are required in many of these personal computers (see Items 1 and 2 in Section 2.0). These two detect multiple pending interrupts from the INS8250-B and test the baud rate. These two conditions were eliminated in the revision part and all parts thereafter. Thus, the more recent UARTs require that one of the following recommendations or a similar change is made to the target system. Changing the software or hardware allows the more recent UARTs to replace the INS8250-B. If the target system services the UART via polling rather than interrupts, then all of the more recent parts will be plug-in replacements for the INS8250-B.

**Note:** The NS16550AF has two pins with new functions (see the data sheet for specifics).

### 6.1 USING THE INS8250A, NS16450, INS82C50A, NS16C450 AND NS16550AF WITH EDGED-TRIGGERED ICUs

Using these UARTs with an edge-triggered ICU as in some of the popular microcomputers requires a signal edge on the INTR pin for each pending UART interrupt. Otherwise, when multiple interrupts are pending the interrupt line will be constantly high active and the edge-triggered ICU will not request additional service for the UART.

### 6.2 CREATING AN INTERRUPT EDGE VIA SOFTWARE

This is done by disabling and then re-enabling UART interrupts via the Interrupt Enable Register (IER) before a specific UART interrupt handling routine (line status errors, received data available, transmitter holding register empty or modem status) is exited. To disable interrupts write H'00 to the IER. To re-enable interrupts write a byte containing ones to the IER bit positions whose interrupts are supposed to be enabled.

### 6.3 CREATING AN INTERRUPT EDGE IN HARDWARE

This is done externally to the UART. One approach is to connect the INTR pin of the UART to the input of an AND gate. The other input of this AND gate is connected to a signal that will always go low active when the UART is accessed (see *Figure 3*). The output of the AND gate is used as the interrupt to the ICU.

**Note:** This simple hardware recommendation will result in one invalid interrupt being generated, so the software routine should be able to handle this. The example shown below was tested using a modified asynchronous card in a few 8088-based microcomputer systems.

## 7.0 Acknowledgements

The editor expresses his gratitude to all of the applications, design and field applications engineers whose laboratory and field research have discovered most of the technical information used in this document.

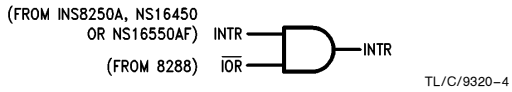



**FIGURE 3. Creating an INTR Edge in Hardware**

## AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

| Symbol | Parameter | Conditions | NS16550AF | | NS16450 NS16C450 | | INS8250A INS82C50A | | INS8250 | | INS8250-B | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{ADS}$ | Address Strobe Width | | 60 | | 60 | | 90 | | 90 | | 120 | | ns |
| $t_{AH}$ | Address Hold Time | | 0 | | 0 | | 0 | | 0 | | 60 | | ns |
| $t_{AR}$ | RD/$\overline{RD}$ Delay from Address | (Note 1) | 30 | | 60 | | 80 | | 110 | | 110 | | ns |
| $t_{AS}$ | Address Setup Time | | 60 | | 60 | | 90 | | 110 | | 110 | | ns |
| $t_{AW}$ | WR/$\overline{WR}$ Delay from Address | (Note 1) | 30 | | 60 | | 80 | | 160 | | 160 | | ns |
| $t_{CH}$ | Chip Select Hold Time | | 0 | | 0 | | 0 | | 0 | | 60 | | ns |
| $t_{CS}$ | Chip Select Setup Time | | 60 | | 60 | | 90 | | 110 | | 110 | | ns |
| $t_{CSC}$ | Chip Select Output Delay from Select | (Notes 1, 8) | | NA | | 100 | | 125 | | 200 | | 200 | ns |
| $t_{CSR}$ | RD/$\overline{RD}$ Delay from Chip Select | (Note 1) | 30 | | 50 | | 80 | | 110 | | 110 | | ns |
| $t_{CSS}$ | Chip Select Output Delay from Strobe | | | NA | | NA | | NA | 0 | 150 | 0 | 150 | ns |
| $t_{CSW}$ | WR/$\overline{WR}$ Delay from Select | (Note 1) | 30 | | 50 | | 80 | | 160 | | 160 | | ns |
| $t_{DH}$ | Data Hold Time | | 30 | | 40 | | 60 | | 60 | | 100 | | ns |
| $t_{DS}$ | Data Setup Time | | 30 | | 40 | | 90 | | 175 | | 350 | | ns |
| $t_{HZ}$ | RD/$\overline{RD}$ to Floating Data Delay | (Notes 3, 8) | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 150 | 0 | 150 | ns |
| $t_{MR}$ | Master Reset Pulse Width | | 5 | | 5 | | 10 | | 10 | | 10 | | $\mu$s |
| $t_{RA}$ | Address Hold Time from RD/$\overline{RD}$ | (Note 1) | 20 | | 20 | | 20 | | 50 | | 50 | | ns |
| $t_{RC}$ | Read Cycle Delay | | 125 | | 175 | | 500 | | 1735 | | 1735 | | ns |
| $t_{RCS}$ | Chip Select Hold Time from RD/$\overline{RD}$ | (Note 1) | 20 | | 20 | | 20 | | 50 | | 50 | | ns |
| $t_{RD}$ | RD/$\overline{RD}$ Strobe Width | | 125 | | 125 | | 175 | | 175 | | 350 | | ns |
| $t_{RDA}$ | RD/$\overline{RD}$ Strobe Delay from $\overline{ADS}$ | | NA | | NA | | NA | | 0 | | 0 | | ns |
| $t_{RDD}$ | RD/$\overline{RD}$ Driver Enable/Disable | (Notes 3, 8) | | 60 | | 60 | | 75 | | 150 | | 250 | ns |
| $t_{RVD}$ | Delay from RD/$\overline{RD}$ to Data | (Note 8) | | 125 | | 125 | | 175 | | 250 | | 300 | ns |
| $t_{WA}$ | Address Hold Time from WR/$\overline{WR}$ | (Note 1) | 20 | | 20 | | 20 | | 50 | | 50 | | ns |
| $t_{WC}$ | Write Cycle Delay | | 150 | | 200 | | 500 | | 1785 | | 1785 | | ns |

**Note 1:** Applicable only when $\overline{ADS}$ is tied low.

**Note 3:** Charge and discharge time is determined by $V_{OL}$, $V_{OH}$ and the external timing.

**Note 8:** Loading of 100 pF.

NA = Not Applicable.

## AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Continued)

| Symbol | Parameter | Conditions | NS16550AF | | NS16450 NS16C450 | | INS8250A INS82C50A | | INS8250 | | INS8250-B | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{WCS}$ | Chip Select Hold Time from WR/$\overline{WR}$ | (Note 1) | 20 | | 20 | | 20 | | 50 | | 50 | | ns |
| $t_{WDA}$ | WR/$\overline{WR}$ Delay from Address | | NA | | NA | | NA | | 50 | | 50 | | ns |
| $t_{WR}$ | WR/$\overline{WR}$ Strobe Width | | 100 | | 100 | | 175 | | 175 | | 350 | | ns |
| $t_{XH}$ | Duration of Clock High Pulse | (Note 4) | 55 | | 140 | | 140 | | 140 | | 140 | | ns |
| $t_{XL}$ | Duration of Clock Low Pulse | (Note 4) | 55 | | 140 | | 140 | | 140 | | 140 | | ns |
| RC | Read Cycle = $t_{AR} + t_{DIW} + t_{RC}$ | | 280 | | 360 | | 755 | | 2000 | | 2205 | | ns |
| WC | Write Cycle = $t_{DDA} + t_{DOW} + t_{WC}$ | | 280 | | 360 | | 755 | | 2100 | | 2305 | | ns |
| **BAUD GENERATOR** | | | | | | | | | | | | | |
| N | Baud Divisor | | 1 | $2^{16}-1$ | 1 | $2^{16}-1$ | 1 | $2^{16}-1$ | 1 | $2^{16}-1$ | 1 | $2^{16}-1$ | ns |
| $t_{BHD}$ | Baud Output Positive Edge Delay | (Note 8) | | 175 | | 175 | | 250 | | 250 | | 250 | ns |
| $t_{BLD}$ | Baud Output Negative Edge Delay | (Note 8) | | 175 | | 175 | | 250 | | 250 | | 250 | ns |
| $t_{HW}$ | Baud Output Up Time | (Note 5) | 75 | | 250 | | 250 | | 330 | | 330 | | ns |
| $t_{LW}$ | Baud Output Down Time | (Note 6) | 100 | | 425 | | 425 | | 425 | | 425 | | ns |
| **RECEIVER** (Note 2) | | | | | | | | | | | | | |
| $t_{RINT}$ | Delay from RD/$\overline{RD}$ (RD RBR/RDLSR) to Reset Interrupt | (Note 8) | | 1000 | | 1000 | | 1000 | | 1000 | | 1000 | ns |
| $t_{RXI}$ | Delay from Read to $\overline{RXRDY}$ Inactive | | | 290 | | NA | | NA | | NA | | NA | ns |
| $t_{SCD}$ | Delay from RCLK to Sample Time | | | 2000 | | 2000 | | 2000 | | 2000 | | 2000 | ns |
| $t_{SINT}$ | Delay from Stop to Set Interrupt | | | 1 RCLK | | 1 RCLK | | 1 RCLK | | 2000 | | 2000 | ns |

**Note 1:** Applicable only when $\overline{ADS}$ is tied low.

**Note 2:** For the NS16550AF in the FIFO Mode (FCR0 = 1) the trigger level and timeout interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive.

**Note 4:** The maximum external clock for the NS16550AF is 8 MHz, NS16450 and INS8250A is 3.1 MHz and INS8250 and INS8250-B is 3.1 MHz. 100 pF load.

**Note 5:** The maximum external clock for the NS16550AF is 8 MHz, NS16450 and INS8250A is 3.1 MHz and INS8250 and INS8250-B is 3.1 MHz. 100 pF load. This parameter is tested on the NS16550AF and guaranteed by design on all other parts.

**Note 6:** The maximum external clock for the NS16550AF is 8 MHz, NS16450 and INS8250A is 2.1 MHz and INS8250 and INS8250-B is 3.1 MHz. 100 pF load. This parameter is tested on the NS16550AF and guaranteed by design on all other parts.

**Note 8:** Loading of 100 pF.

NA = Not Applicable.

## AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Continued)

| Symbol | Parameter | Conditions | NS16550AF | | NS16450 NS16C450 | | INS8250A INS82C50A | | INS8250 | | INS8250-B | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| **TRANSMITTER** | | | | | | | | | | | | | |
| $t_{HR}$ | Delay from WR/$\overline{WR}$ (WR THR) to Reset Interrupt | (Note 8) | | 175 | | 175 | | 1000 | | 1000 | | 1000 | ns |
| $t_{IR}$ | Delay from RD/$\overline{RD}$ (RD IIR) to Reset Interrupt (THRE) | (Note 8) | | 250 | | 250 | | 1000 | | 1000 | | 1000 | ns |
| $t_{IRS}$ | Delay from Initial INTR Reset to Transmit Start | (Note 10) | 8 | 24 | 24 | 40 | 24 | 40 | | 16 | | 16 | Baudout Cycles |
| $t_{SI}$ | Delay from Initial Write to Interrupt | (Notes 7, 9) | 16 | 24 | 16 | 24 | 16 | 24 | | 50 | | 50 | Baudout Cycles |
| $t_{SS}$ | Delay from Stop to Next Start | | | NA | | NA | | NA | | 1000 | | 1000 | ns |
| $t_{STI}$ | Delay from Stop to Interrupt (THRE) | (Note 7) | 8 | 8 | 8 | 8 | 8 | 8 | | 8 | | 8 | Baudout Cycles |
| $t_{SXA}$ | Delay from Start to TXRDY Active | (Note 8) | | 8 | | NA | | NA | | NA | | NA | Baudout Cycles |
| $t_{WXI}$ | Delay from Write to TXRDY Inactive | (Note 8) | | 195 | | NA | | NA | | NA | | NA | ns |
| **MODEM CONTROL** | | | | | | | | | | | | | |
| $t_{MDO}$ | Delay from WR/$\overline{WR}$ (WR MCR) to Output | (Note 8) | | 200 | | 200 | | 1000 | | 1000 | | 1000 | ns |
| $t_{RIM}$ | Delay to Reset Interrupt from RD/$\overline{RD}$ (RD MSR) | (Note 8) | | 250 | | 250 | | 1000 | | 1000 | | 1000 | ns |
| $t_{SIM}$ | Delay to Set Interrupt from MODEM Input | (Note 8) | | 250 | | 250 | | 1000 | | 1000 | | 1000 | ns |

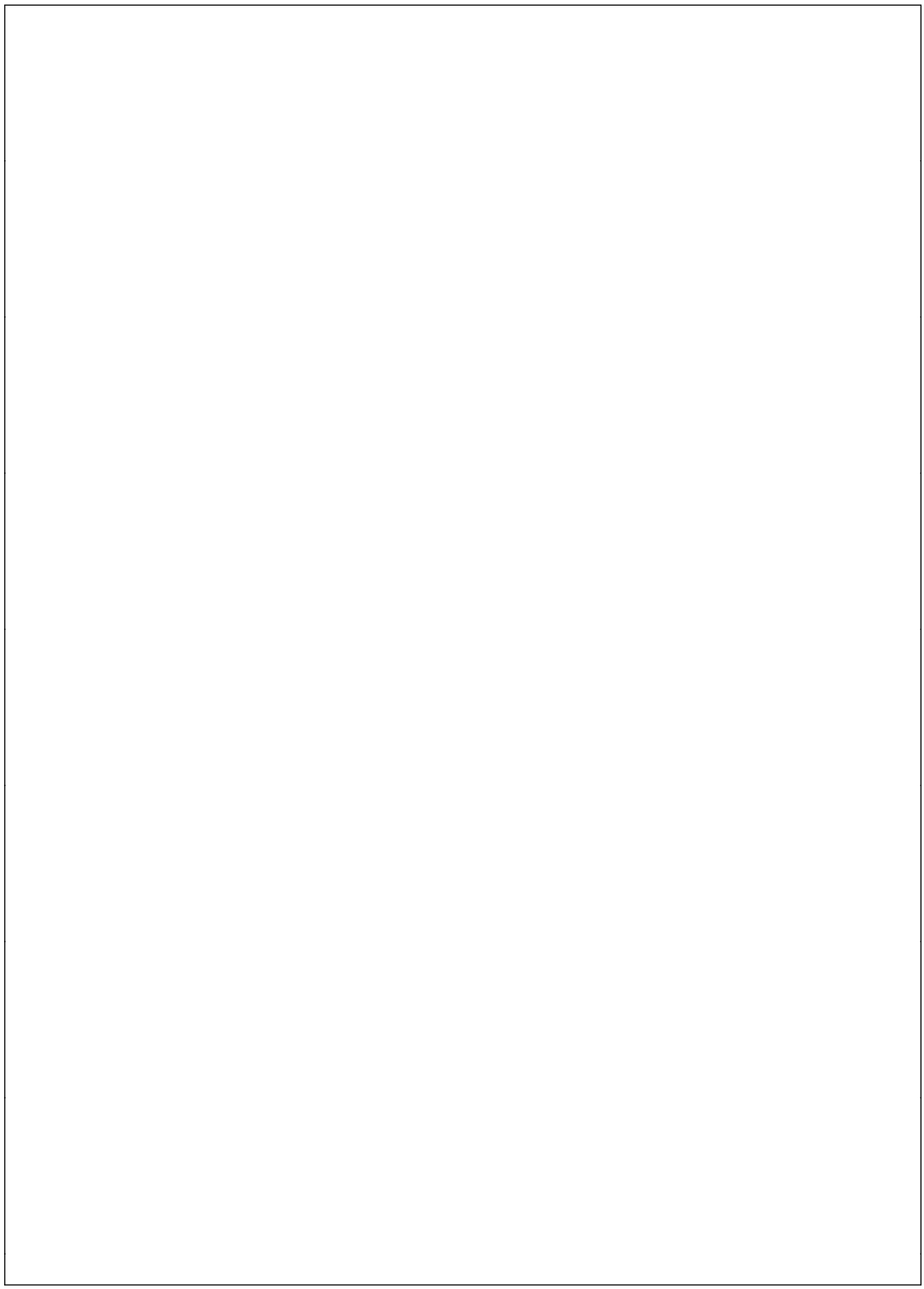
**Note 7:** This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active.

**Note 8:** Loading of 100 pF.

**Note 9:** For both the NS16C450 and INS82C50A the value of $t_{SI}$ will range from 16 to 48 baudout cycles.

**Note 10:** For both the NS16C450 and the INS82C50A the value of $t_{IRS}$ will range from 24 to 40 baudout cycles.

NA = Not Applicable.



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**National Semiconductor Corporation**
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

**National Semiconductor Europe**
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**
Tel: 81-043-299-2309
Fax: 81-043-299-2408